Claims:

1. An apparatus for conditional branching comprising:

a sequencer executing a plurality of program instructions, one or more of said program instructions including a conditional branch instruction, said conditional branch instruction specifying a branch condition address and a conditional instruction,

a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory, a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction.

2. An apparatus as recited in claim 1 and further comprising a plurality of said branch units and further comprising an operator that accepts a respective plurality of said branch flags and logically combines said branch flags to create a branching bit, said branching bit indicating whether said sequencer is to branch according to said conditional instruction.

3. An apparatus as recited in claim 1, said flag selection memory comprising a plurality of programmable registers.

4. An apparatus as recited in claim 1, said first flag selectors comprising a multiple input, single output multiplexer.

5. An apparatus as recited in claim 1, said second flag selector comprising a multiple input single out multiplexer.

6. An apparatus as recited in claim 2, said operator comprising a multiple input logical AND operator.

7. An apparatus as recited in claim 1, wherein said branch address comprises a plurality of bits in said conditional branch instruction.

8. An apparatus as recited in claim 1 and further comprising a b1not0 bit in said conditional branch instruction directing said sequencer whether it is to branch on a one or a zero of said branch flag.

9. An apparatus as recited in claim 2 and further comprising a b1not0 bit in said conditional branch instruction directing said sequencer whether it is to branch on a one or a zero of said branch flag.

10. An apparatus as recited in claim 9 and further comprising a dual input selector accepting said branching bit and an inverse of said branching bit, said b1not0 bit operating on said dual input selector.

11. An apparatus as recited in claim 10, wherein said dual input selector is a dual input single output multiplexer.

12. A method for compiling source code containing one or more conditional branching instructions comprising the steps of:

interpreting the source code, the source code comprising a plurality of program instructions,

identifying each conditional branch instruction in said source code, and for each conditional branching instruction, determining a set of flags upon which said conditional branching instruction is based, identifying a flag selection register value for each flag in said set of flags, and storing each said flag selection register value in a respective one of a plurality of flag selection register array elements, assigning a branch condition address for said conditional branching instruction, encoding said branch condition address in a binary representation of said conditional branching instruction, and storing said encoded one or more conditional branching instructions and said flag selection register array elements in an object code format.

13. A method for compiling source code as recited in claim 12, the step of identifying each conditional branching instruction further comprising the step of re-ordering said set of flags to a set placement format.

14. A method for compiling source code as recited in claim 12 and further comprising the step of converting all disjunctive operations to a conjunctive equivalent.

15. An apparatus for conditional branching comprising:

a compiler for converting source code including one or more conditional branch instructions into object code, the compiler assigning values for a branch condition address and values for a flag selection memory,

a sequencer executing said object code comprising one or more of said conditional branch instructions, each said conditional branch instruction specifying a branch condition address and a conditional instruction, and

a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory, a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction.

16. An apparatus for conditional branching as recited in claim 15, said compiler also converting disjunctive logical operations specified in said conditional branch instructions to an equivalent conjunctive logical operation.

17. An apparatus for conditional branching as recited in claim 16, said compiler setting a b1not0 bit for said program instruction if said logical operation is converted from said disjunctive logical operation to said equivalent conjunctive logical operation.

18. An apparatus for conditional branching as recited in claim 15, and further comprising one or more arithmetic logic units that supply said plurality of available flags.